



Features

- Compliant with QSFP28 Standard: SFF-8661 Revision 1.9, SFF-8636 Revision 2.10a
- Compliant with 100G 4WDM-40 MSA technical specification rev 1.0
- High speed I/O electrical interface (CAUI-4) compliant with IEEE 802.3-2018
- Single 3.3V Supply Voltage
- Maximum power consumption 4.5W
- 0-70 °C Case Operating Temperature
- LAN WDM EML laser and APD Receiver Array
- QSFP28 MSA package with duplex LC connector
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Class 1 Laser

Absolute Maximum Ratings

Table 1 – Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Storage Temperature	T_s	-40	-	+85	°C	
Supply Voltage	V_{CC}	-0.3	-	3.6	V	
Relative Humidity (non-condensing)	RH	5	-	95	%	
Data Input Voltage – Differential	$ V_{DIP}-V_{DIN} $	-	-	1.0	V	
Control Input Voltage	V_I	-0.3	-	$V_{CC}+0.5$	V	
Control Output Current	I_o	-20	-	20	mA	

Recommended Operating Conditions

Table 2 – Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T _{OPR}	0	-	70	°C	
Power Supply Voltage	V _{CC}	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	I _{CC_IP}	-	-	1800	mA	
Sustained peak current at hot plug	I _{CC_SP}	-	-	1485	mA	
Maximum Power Dissipation	P _D	-	-	4.5	W	
Maximum Power Dissipation, Low Power Mode	P _{DLP}	-	-	1.5	W	
Aggregate Bit Rate	ABR	-	103.125	-	Gb/s	
Data Rate per Lane	DRL	-	25.78	-	Gb/s	
Control Input Voltage High	V _{IH}	V _{CC} *0.7	-	V _{CC} +0.3	V	
Control Input Voltage Low	V _{IL}	-0.3	-	V _{CC} *0.3	V	
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Module power supply noise tolerance 10 Hz - 10 MHz (peak-to-peak)	-	-	-	66	mVpp	
Rx Differential Data Output Load	-	-	100	-	ohms	
Operating Distance	-	2	-	40000	m	With FEC

Optical and Electrical Characteristics

Table 3 – Transmitter Optical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength L0	λ_{C0}	1294.53	1295.56	1296.59	nm	
Wavelength L1	λ_{C1}	1299.02	1300.05	1301.09	nm	
Wavelength L2	λ_{C2}	1303.54	1304.58	1305.63	nm	
Wavelength L3	λ_{C3}	1308.09	1309.14	1310.19	nm	
Side-mode suppression ratio	SMSR	30			dB	
Total Average Optical Launch Power	P_{OUT}	-	-	12.5	dBm	
Average Launch Power Tx_Off (Each Lane)	P_{OUT_OFF}	-	-	-30	dBm	
Average Optical Launch Power (Each Lane)	P_{OUTL}	-2.5	-	6.5	dBm	
Extinction Ratio	ER	4.5	-	-	dB	
Optical Modulation Amplitude (Each Lane)	OMA	0.5	-	6.5	dBm	
Launch Power in OMA minus TDP (Each Lane)	OMA-TDP	-0.5	-	-	dBm	
Difference in launch power between any two lanes (Average and OMA)	DT_OMA	-	-	4	dB	
Transmitter and Dispersion Penalty (Each Lane)	TDP	-	-	3	dB	
Optical Return Loss Tolerance	ORLT	20	-	-	dB	
Transmitter Eye Mask Definition	-	{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				
Transmitter Reflectance	TR	-	-	-26	dB	

Table 4 – Receiver Optical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength L0	λ_{C0}	1294.53	1295.56	1296.59	nm	
Wavelength L1	λ_{C1}	1299.02	1300.05	1301.09	nm	
Wavelength L2	λ_{C2}	1303.54	1304.58	1305.63	nm	
Wavelength L3	λ_{C3}	1308.09	1309.14	1310.19	nm	
Receiver sensitivity (OMA), each lane at 5 x 10 ⁻⁵ BER		-	-	-18.5	dBm	
Stressed receiver sensitivity (OMA), each lane, each lane at 5 x 10 ⁻⁵ BER	-	-	-	-16	dBm	
Stressed Receiver Sensitivity Test Conditions:						
Stressed Eye J2 Jitter (Each Lane)	-	-	0.33	-	UI	
Stressed Eye J4 Jitter (Each Lane)	-	-	0.48	-	UI	
Vertical Eye Closure Penalty	-	-	2.5	-	dB	
SRS eye mask definition { X1, X2, X3, Y1, Y2, Y3}		{0.39, 0.5, 0.5, 0.39, 0.39, 0.4}				
Damage threshold, each lane	$P_{in, damage}$	-2.5	-	-	dBm	
Average Receive Power (Each Lane)	-	-20.5	-	-3.5	dBm	
Receive Power in OMA (Each Lane), Overload	OMA	-	-	-3.5	dBm	
Receiver Reflectance	RX_R	-	-	-26	dB	

Table 5 – Electrical Specifications

High-Speed Signal: Compliant to CAUI-4 (IEEE 802.3bm)

Low-Speed Signal: Compliant to SFF-8679

Transmitter (Module Input)						
Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Signaling rate per lane (range)		25.78125 ± 100 ppm			GBd	
Differential pk-pk input voltage tolerance	V _{IN,P-P}	900	-	-	mVpp	
Differential Termination Mismatch		-	-	10	%	
Single-ended voltage tolerance range		-0.4	-	3.3	V	
DC common mode voltage		-350	-	2850	mV	
Receiver (Module Output)						
Signaling rate per lane (range)		25.78125 ± 100 ppm			GBd	
AC common-mode output voltage		-	-	17.5	mV	
Differential output voltage	V _{OUT,P-P}	-	-	900	mVpp	
Eye width		0.57	-	-	UI	
Eye height, differential		228	-	-	mV	
Vertical eye closure		-	-	5.5	dB	
Differential Termination Mismatch		-	-	10	%	
Output Rise/Fall Time, 20%~80%	T _R	12	-	-	ps	
DC common mode voltage		-350	-	2850	mV	

Timing

Table 6 –Timing for QSFP+ Soft Control and Status Functions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Initialization Time	t_init	-	-	10	s	
Reset Init Assert Time	t_reset_init	10	-	-	µs	
Serial Bus Hardware Ready Time	t_serial	-	-	2000	ms	
Monitor Data Ready Time	t_data	-	-	2000	ms	
Reset Assert Time	t_reset	-	-	10	s	
LPMode/TxDis mode change time	t_LPMode/TxDis	-	-	100	ms	
LPMode Assert Time	ton_LPMode	-	-	100	ms	
LPMode De-assert Time	toff_LPMode	-	-	10	s	
IntL/RxLOSL mode change time	t_IntL/RxLOSL	-	-	100	ms	
IntL Assert Time	ton_IntL	-	-	200	ms	
IntL Deassert Time	toff_IntL	-	-	500	µs	
RxLOSL Assert Time (Optional Fast Mode)	ton_f_LOS	-	-	1	ms	
RxLOSL Deassert Time (Optional Fast Mode)	toff_f_LOS	-	-	3	ms	
Rx LOS Assert Time	ton_lol	-	-	100	ms	
Tx Fault Assert Time	ton_Txfault	-	-	200	ms	
Flag Assert Time	ton_flag	-	-	200	ms	
Mask Assert Time	ton_mask	-	-	100	ms	
Mask Deassert Time	toff_mask	-	-	100	ms	
Application or Rate Select Change Time	t_ratesel	-	-	N/A	ms	
Power_over-ride or Power-set Assert Time	ton_Pdown	-	-	100	ms	
Power_over-ride or Power-set De-assert Time	toff_Pdown	-	-	10	s	

Table 7 –I/O Timing for Squelch & Disable

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Rx Squelch Assert Time	ton_Rxsq	-	-	15	ms	
Rx Squelch Deassert Time	toff_Rxsq	-	-	15	ms	
Tx Squelch Assert Time	ton_Txsq	-	-	400	ms	
Tx Squelch Deassert Time	toff_Txsq	-	-	400	ms	
Tx Disable Assert Time	ton_txdis	-	-	100	ms	
Tx Disable Deassert Time	toff_txdis	-	-	400	ms	
Tx Disable Assert Time (Optional Fast Mode)	Ton_f_TxDis	-	-	3	ms	

Tx Disable Deassert Time (Optional Fast Mode)	Toff_f_TxDi s	-	-	10	ms	
Rx Output Disable Assert Time	ton_rxdis			100	ms	
Rx Output Disable Deassert Time	toff_rxdis			100	ms	
Squelch Disable Assert Time	ton_sqdis			100	ms	
Squelch Disable Deassert Time	toff_sqdis			100	ms	

Table 8 – Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	°C	Internal
Voltage	0 to V _{CC}	±3%	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each Lane)	-2.5 to 6.5	±3	dB	Internal
Rx Power (Each Lane)	-20.5 to -3.5	±3	dB	Internal

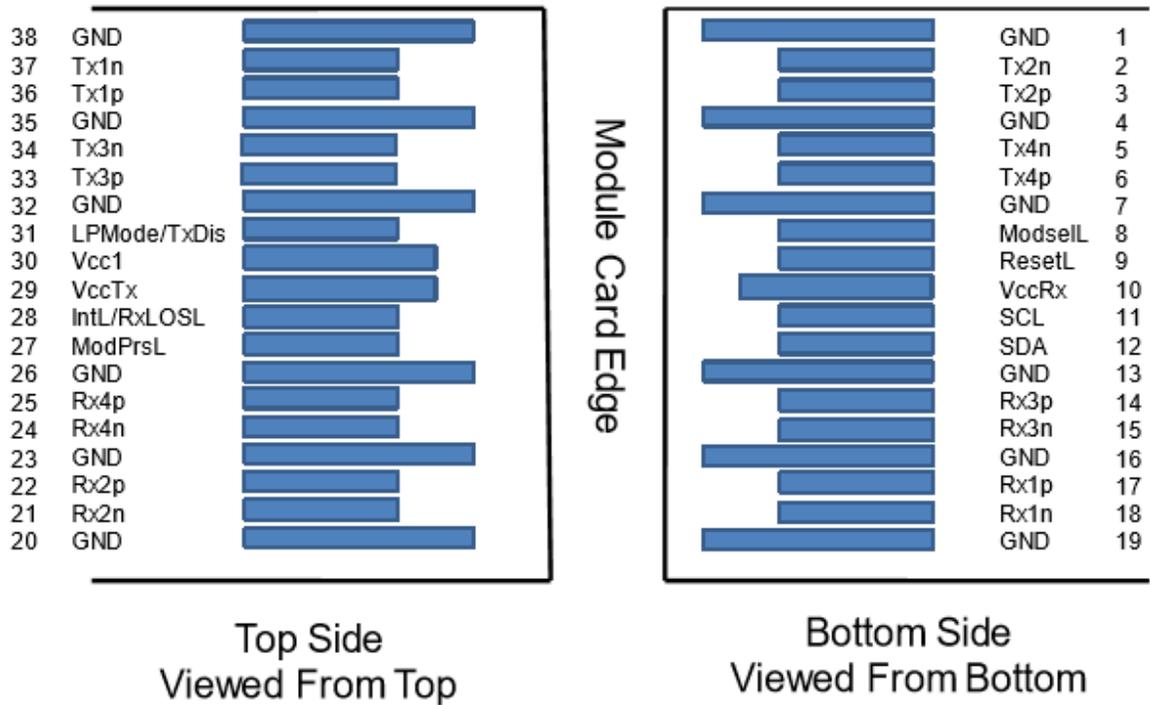
Table 9 – Pin Definitions

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/RxL OS L	Interrupt. Optionally configurable as RxLOSL via the management interface (SFF-8636).	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode/ TxDis	Low Power Mode. Optionally configurable as TxDis via the management interface (SFF-8636).	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, Vcc1 and VccTx are applied concurrently and may be internally connected within the module in any combination. Vcc contacts in SFF-8662 and SFF-8672 each have a steady state current rating of 1 A.

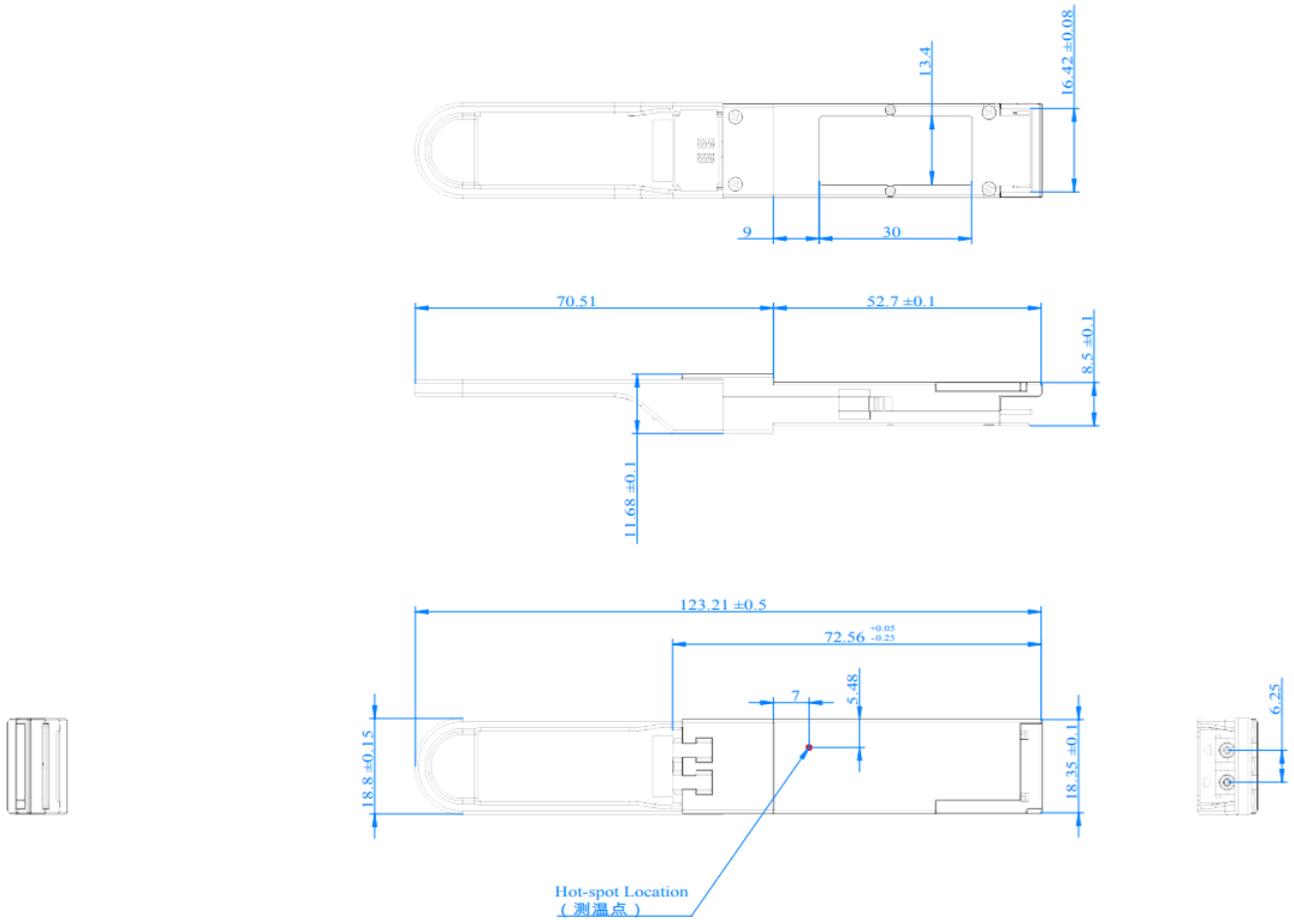
QSFP+ Module Pad Layout



Recommended Host Board Power Supply Filtering

See SFF-8679

Mechanical Diagram



Order Information

Table 10 – Order Information

Part No.	Application	Data Rate	Laser Source	Fiber Type
SPQ-CE-ER-CDFN	100G 4WDM-40	103.125 Gb/s	LAN WDM EML	SMF

Warnings

Handling Precautions: This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

Laser Safety: Class 1 Laser Product. Complies with FDA performance standards for laser products except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019. Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.

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